FORM PTO-1390 U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 2729-055

U.S. APPLIC. NO. (if known, see 37 CFR 1.5): 09/202902 Not Yet Assigned

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/KR98/00091	17 April 1998	22 April 1997

TITLE OF INVENTION

METHOD OF DRIVING SURFACE DISCHARGE PLASMA DISPLAY PANEL

APPLICANT(S) FOR DO/EO/US

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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. [] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. [] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. [X] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [X] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau.
   c. [] is not required, as the application was filed in the United States Receiving Office (RO/US)

6. [] A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. [] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [] have been transmitted by the International Bureau.
   c. [] have not been made; however, the time limit for making such amendment has **NOT** expired.
   d. [] have not been made and will not be made.

8. [] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. [] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. [X] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. [] A FIRST preliminary amendment.
    [] A SECOND or SUBSEQUENT preliminary amendment.

14. [] A substitute specification.

15. [X] A change of power of attorney and/or address letter.

16. [X] Other items or information.
    PCT/ISA/220
    PCT/ISA/210 International Search Report
    PCT/IB/308

U.S. APPLIC. NO. (if known, see 37 CFR 1.50)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
Not Yet Assigned	PCT/KR98/00091	2729-055

	CALCULATIONS	PTO USE ONLY
17. [X] The following fees are submitted:		
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO $840.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) $670.00 No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $760.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $970.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0.00	

Claims	Number Filed	Number Extra	Rate		
Total Claims	2 -20 =	0	x $18.00	$ 0.00	
Independent Claims	1 -3 =	0	x $78.00	$ 0.00	
Multiple dependent claim(s) (if applicable)			+ $260.00	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 840.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$ 0.00	
SUBTOTAL =				$ 840.00	
Processing fee of $130.00 for furnishing the English translation later than the [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$ 0.00	
TOTAL NATIONAL FEE =				$ 840.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$40.00	
TOTAL FEES ENCLOSED =				$ 880.00	
				Amount to be: refunded	$
				charged	$

a. [X] A check in the amount of $ 880.00 to cover the above fees is enclosed.

b. [] Please charge my Deposit Account No. in the amount of $ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 07-1337. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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PATENT

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In re Application of	:	
S. KIM et al.	:	
Serial No. Not Yet Assigned	:	Group Art Unit: Unknown
Filed: December 22, 1998	:	Examiner: Unknown

For: METHOD OF DRIVING SURFACE DISCHARGE PLASMA DISPLAY PANEL

CORRESPONDENCE ADDRESS CHANGE

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

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METHOD OF DRIVING SURFACE DISCHARGE PLASMA DISPLAY PANEL

Technical Field

The present invention relates to a method of driving a surface discharge plasma display panel, and more particularly, to a method for driving a three-electrode surface-discharge alternating-current plasma display panel(AC PDP).

Background Art

FIG. 1 shows an electrode pattern of a conventional surface discharge plasma display panel. FIG. 2 is a schematic sectional view of a pixel of FIG. 1. Referring to FIGS. 1 and 2, the conventional surface discharge plasma display panel includes address electrodes A1, A2, A3, ..., Am, a first dielectric 21, a luminescent material 22, scan electrodes Y1, Y2, ...,Yn-1, Yn, 231, 232, common electrodes X, 241, 242, a second dielectric 25, and a protective layer 26. Each of the scan electrodes Y1, Y2, ..., Yn-1, Yn, includes an indium tin oxide (ITO) scan electrode 231 and a bus scan electrode 232. In the same manner, each of the common electrodes X, 241, 242 includes a common ITO electrode 241 and a common bus electrode 242. Gas for forming plasma is sealed between the protective layer 26 and a first dielectric 21.

The address electrode A1, A2, A3,..., Am are coated on a lower substrate (not shown) of a first substrate in a predetermined pattern. The first dielectric 21 is coated on the address electrodes A1, A2, A3, ..., Am. The luminescent material 22 is coated on the first dielectric 21 in a predetermined pattern. Depending on circumstances, without forming the first dielectric 21, the luminescent material 22 may be coated on the address electrodes A1, A2, A3, ..., Am, in a predetermined pattern. The scan electrodes Y1, Y2, ..., Yn-1, Yn, 231, 242 and the common electrodes X, 241, 242 are formed on an upper substrate (not shown) of a second substrate, such that they intersect with the address electrodes A1, A2, A3, ..., Am. The respective intersections each define a corresponding pixel. The second dielectric 25 is coated on the scan electrodes Y1, Y2, ..., Yn-1, Yn, 231, 232 and the common electrodes X, 241, 242. The protective layer 26 for protecting the

panel from a strong electrical field is coated on the second dielectric 25.

In the prior art driving method of a surface discharge plasma display panel, a relatively high voltage is applied between the scan electrodes Y1, Y2, ..., Yn-1, Yn, 231, 232 and the common electrodes X, 241, 242 to accumulate wall charges in the respective pixel by a surface discharge, and the wall-charges accumulated by the surface discharge are removed, in a resetting step. The conventional driving method is disclosed in U.S. Patent No. 5,446,344.

FIG. 3 is for illustrating a conventional driving method of a surface discharge plasma display panel.

In a first reset interval (a-b), a pulse of voltage Vaw, a pulse of voltage Vs+Vw, and 0 V are applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn, respectively. Here, the voltage Vs+Vw obtained by adding the voltage Vw to the scan voltage Vs is higher than the voltage Vaw. Accordingly, a relatively high voltage Vs+Vw is applied between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn, so that a surface discharge occurs between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn ('a' of FIG. 3). And then, positive(+) wall-charges are accumulated in the positive layer 26 of FIG. 2 under each of the scan electrodes 231, 232 of FIG. 2, and negative(-) wall-charges are accumulated in the positive layer 26 under the common electrodes 241, 242 of FIG. 2.

The voltage of the wall-charges accumulated during the first reset interval (a-b) is a re-dischargeable voltage. In a second reset interval (b-c), 0 V is applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn. Accordingly, due to the wall-charges accumulated during the first reset interval (a-b), a surface discharge occurs between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn. And then, the wall-charges of all pixels are removed.

In an address step, in a state in which a pulse of voltage Vax is applied to the common electrodes X, scan pulses of a voltage -Vy are sequentially applied to each of the scan electrodes Y1, Y2, ..., Yn. When the scan pulse is not applied, a negative voltage -Vsc which is a level lower than the voltage -Vy of the scan pulse is applied. When a pulse of the address voltage Va is applied to an address

electrode Am selected while the scan pulse is applied to a scan electrode Y1, Y2, ..., Yn, for example, during interval (c-d) for the scan electrode Y1, a facing discharge is performed in a corresponding pixel. This is because a voltage for facing discharge Va+Vy is applied between the corresponding scan electrode Y1, Y2, ..., or Yn and the selected address electrode Am. At this time, when a negative voltage -Vsc which is lower than the voltage -Vy of the scan pulse is applied, the facing discharge stops. And then, positive(+) wall-charges are accumulated under the scan electrodes 231, 232 of the selected pixel.

In a first sustaining discharge interval (g-h), a a pulse of the voltage Vs/2 which is ½ the scan voltage Vs, 0V, and a a pulse of the sustaining discharge voltage Vs, are applied to the address electrodes Am, the common electrode X, and the scan electrodes Y1, Y2, ..., Yn, respectively. That is, in a state in which positive(+) wall-charges are accumulated under the scan electrode Y1, Y2, ..., or Yn of the selected pixel, when a relatively high negative-voltage is applied between the scan electrodes Y1, Y2, ..., Yn and the common electrodes X, a surface discharge occurs in the selected pixel. When the surface discharge is performed in the selected pixel, plasma is formed in a gas layer of a corresponding region, and a luminescent material 22 of FIG. 2 is excited by an UV-ray to emit light.

In a second sustaining discharge interval (i-j), a a pulse of the voltage Vs/2 which is ½ the scan voltage Vs, a a pulse of the sustaining discharge voltage Vs, and 0V, are applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ...,Yn, respectively. That is, in a state in which wall-charges are accumulated, when a relatively high negative voltage is applied between the scan electrodes Y1, Y2, ..., Yn and the common electrodes X, a surface discharge occurs in a selected pixel. And then, positive(+) wall-charges are accumulated under the scan electrodes 231, 232 of the selected pixel, and negative(-) wall-charges are accumulated under the common electrodes 241, 242. When the surface discharge is performed in the selected pixel, plasma is formed in a gas layer of a corresponding region, and a luminescent material 22 is excited by a UV-ray to emit light. The operations of the first and second sustained discharge intervals are repeated during the sustaining discharge period, to thereby

maintain the emission of light at the selected pixel.

In the conventional driving method, in the resetting step (interval a-c of FIG. 3), a pulse of a relatively high voltage Vs+Vw is applied between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn, so that a surface discharge occurs. Accordingly, the light of relatively high brightness is emitted from the unselected pixels, to thereby decrease the contrast of a display screen.

Disclosure of Invention

It is an object of the present invention to provide a driving method of a surface discharge plasma display panel for emitting the light of relatively low brightness from the pixels unselected in each sub-field.

To accomplish the above object of the present invention, a driving method of a surface discharge plasma display panel is adopted to a surface discharge plasma display panel having a first substrate and a second substrate space apart and facing each other, and common electrodes, scan electrodes, and address electrodes arranged between said first and second substrates, said common electrodes being arranged in parallel with said scan electrodes, said address electrodes being arranged orthogonal to said common electrodes and said scan electrodes to form respective intersections which each define a corresponding pixel.

The driving method of a surface discharge plasma display panel comprises a reset step, an address step, and a sustaining discharging step. In the reset step, a first voltage is applied between the scan electrodes and the address electrodes to accumulate wall charges in the respective pixel by a facing discharge, and the wall-charges accumulated by the facing discharge are removed. In the address step, a second voltage is applied between a corresponding scan electrodes and selected address electrodes so that a facing discharge occurs, to form wall-charges in the selected pixels. In the sustaining discharge step, a third alternating-current voltage is applied between the scan electrodes and the common electrodes so that a surface discharge occurs in the selected pixels.

In the reset step of the present invention, the wall charges to be removed are accumulated by the facing discharge. Accodingly, the light of relatively low brightness is emitted from the pixels unselected in each sub-field.

Preferably, the reset step includes a first, a second and a third reset step. In the first reset step, a fourth voltage is applied between the scan electrodes and the common electrodes, and thereby remove remnant wall-charges from a previous sub-field, said fourth voltage has an opposite polarity to a voltage applied last in the sustained discharging step. In the second reset step, said first voltage is applied between the scan electrodes and the address electrodes, and thereby cause the facing discharge. In the third reset step, a fifth voltage is applied between the scan electrodes and the address electrodes, and thereby remove wall-charges accumulated by the facing discharge, said fifth voltage has an opposite polarity to said first volatge and lower than said first voltage. Also, the third reset step is shorter than the first and second reset steps. And, the third reset step is repeated.

Brief Description of Drawings

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a diagram showing a typical electrode pattern of a surface discharge plasma display panel;

FIG. 2 is a schematic sectional view of a pixel of the pattern of FIG.1;

FIG. 3 is a diagram showing voltage waveforms applied to electrodes according to a plasma display panel driving method based on a prior art.

FIG. 4 is a diagram showing voltage waveforms applied to electrodes according to a plasma display panel driving method based on an embodiment of the present invention.

FIG. 5 is a diagram showing the state of a selected pixel during a last sustaining discharge interval (O-P) of FIG. 4;

FIG. 6A is a disgram showing the state of a unit pixel in a first reset interval (A-B) of FIG. 4;

FIG. 6B is a diagram showing the state of a unit pixel during a second reset interval (C-D) of FIG. 4; and

FIG. 6C is a diagram showing the state of a unit pixel in a third reset interval (E-F) of FIG. 4.

FIG. 7 is a diagram showing the state of a pixel selected during an address interval (G-K) of FIG. 4.

FIG. 8A is a diagram showing the state of a pixel selected during a first sustaining discharge interval (K-L) of FIG 4

FIG. 8B is a diagram showing the state of a pixel selected during a second sustaining discharge interval (M-N) of FIG. 4

FIG. 9 is a diagram showing voltage waveforms applied to electrodes according to a plasma display panel driving method based on the other embodiment of the present invention.

Best Mode for Carrying Out the Invention

FIG. 4 shows the voltage waveforms applied to electrodes according to a plasma display panel driving method based on an embodiment of the present invention. Referring to FIG. 4, In the reset interval (A-G), a first voltage Vw is applied between the scan electrodes Y1, Y2, ..., Yn and the address electrodes Am to accumulate wall charges in the respective pixel by a facing discharge, and the wall-charges accumulated by the facing discharge are removed. In the address interval (G-K), a second voltage Va+Vk+Vy is applied between a corresponding scan electrodes Y1, Y2, ..., Yn and selected address electrodes Am so that a facing discharge occurs, to form wall-charges in the selected pixels. In the sustaining discharge interval(K-Q), a third alternating-current voltage Vs+Vk is applied between the scan electrodes Y1, Y2, ..., Yn and the common electrodes X so that a surface discharge occurs in the selected pixels.

In the reset interval (A-G) of this embodiment, the wall charges to be removed are accumulated by the facing discharge. Accodingly, the light of relatively low brightness is emitted from the pixels unselected in each sub-field. Also, there are residual wall charges on the address electrodes Am in the reset interval (A-G), and thereby the second voltage Va+Vk+Vy applied in the address

interval (G-K) can be lowered.

Three steps are sequentially performed in the reset interval (A-G). In the first reset step (interval A-B), a fourth voltage Vs+Vk is applied between the scan electrodes Y1, Y2, ..., Yn and the common electrodes X, and thereby remove remnant wall-charges from a previous sub-field, the fourth voltage Vs+Vk has an opposite polarity to a voltage applied last in the sustained discharging interval (K-Q). In the second reset step (interval C-D), the first voltage Vw is applied between the scan electrodes Y1, Y2, ..., Yn and the address electrodes Am, and thereby cause the facing discharge. In the third reset step (interval E-F), a fifth voltage Vk is applied between the scan electrodes Y1, Y2, ..., Yn and the address electrodes Am, and thereby remove wall-charges accumulated by the facing discharge, the fifth voltage Vk has an opposite polarity to the first volatge Vw and lower than the first voltage Vw. The third reset interval (E-F) is shorter than the first (A-B) and second (C-D) reset intervals. Also, the third reset step (interval E-F) is repeated.

A driving method of FIG. 4 is adopted for the case that 0V, a negative(-) voltage -Vk of a relatively high level, for example, -140V, and a positive(+) voltage Vs of a relatively low level, for example, 40V, are applied to address electrodes Am, common electrodes X, and scan electrodes Y1, Y2, ..., Yn, respectively. Here, negative(-) wall-charges are accumulated under the scan electrodes 231, 232 of a selected pixel, and positive(+) wall-charges are accumulated under the common electrodes 241, 242, as shown in FIG. 5. Reference numerals of FIG. 5 which are the same as those of FIG. 2 indicate identical elements. Meanwhile, wall-charges are not accumulated in unselected pixel regions.

In the first reset interval (A-B), 0V, a pulse of the positive(+) voltage Vs, and a pulse of the negative(-) voltage -Vk are applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn, respectively. That is, in a state in which the voltage of the address electrodes Am is maintained at 0V, a voltage applied between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn is a negative voltage Vs+Vk of the voltage -(Vs+Vk) of a final sustaining discharge interval of a previous sub-field. Accordingly, the wall-charges in the pixels selected in a previous sub-field are removed. Also, as shown in FIG. 6A, positive(+) wall-charges are accumulated in a protective layer

26 under each of the scan electrodes 231, 232 of the pixel selected in the previous sub-field, and negative(-) wall-charges are accumulated in the protective layer 26 under the common electrodes 241, 242. Reference numerals of FIG. 6A which are the same as those of FIG. 2 indicate identical elements. Meanwhile, wall-charges are not accumulated in a pixel region not selected from the previous sub-field.

In the second reset interval (C-D), 0V, a a pulse of the positive(+) voltage Vs, and a a pulse of the positive(+) voltage Vw for facing discharge, for example, 180 V, are applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn, respectively. That is, the relatively high voltage Vw is applied between the address electrodes Am and the scan electrodes Y1, Y2, ..., Yn. Accordingly, a facing discharge occurs between the address electrodes Am of pixels where wall-charges are accumulated in the first reset interval (A-B), that is, the pixels selected from the previous sub-field, and the scan electrodes Y1, Y2, ..., Yn. Meanwhile, a facing discharge does not occur between the address electrodes Am of pixels where wall-charges are not accumulated in the first reset interval (A-B), that is, the pixels not selected from the previous sub-field, and the scan electrodes Y1, Y2, ..., Yn. As shown in FIG. 6B, negative(-) wall-charges are accumulated in the protective layer 26 under the scan electrodes 231, 232 of each pixel selected from the previous sub-field, and the positive(+) wall-charges are accumulated in a luminescent material 22 of the address electrodes Am. Here, positive(+) wall-charges are accumulated in the protective layer 26 under the common electrodes 241, 242. Reference numerals of FIG. 6B which are the same as those of FIG. 2 indicate identical elements. Meanwhile, wall-charges are not accumulated in a pixel region not selected from the previous sub-field.

In the third reset interval (E-F), 0 V is applied to the address electrodes Am and the common electrodes X, and a pulse of the negative(-) voltage -Vk is applied to the scan electrodes Y1, Y2, ..., Yn. The operation of the third reset interval is performed relatively quickly, so that the pulse width of the negative(-) voltage -Vk applied to the scan electrodes Y1, Y2, ..., Yn, is relatively short. As shown in FIG. 4, the operation of the third reset interval (E-F) is sequentially

performed again. Accordingly, as shown in FIG. 6C, the wall-charges of the pixels selected from the previous sub-field are removed. Nevertheless, there are residual wall charges on the address electrodes Am in the reset interval (A-G), and thereby the second voltage Va+Vk+Vy applied in the address interval (G-K) can be lowered. Reference numerals of FIG. 6C which are the same as those of FIG. 2 indicate identical elements.

Then, in the address period (G-K), in a state in which a pulse of the positive(+) voltage Vs is applied to the common electrodes X, scan pulses of the negative voltage -Vk-Vy higher than the negative(-) voltage -Vk, for example, -180V, are sequentially applied to each of the scan electrodes Y1, Y2, ..., Yn. When the scan pulse is not applied, a negative voltage -Vp lower than the negative(-) voltage -Vk, is applied. When an address voltage Va, for example, 80V, is applied to an address electrode Am selected while the scan pulse is applied to one of the corresponding scan electrodes Y1, Y2, ..., or Yn, for example, G-H interval for the scan electrode Y1, facing discharge occurs in a corresponding pixel. This is because a voltage for facing discharge Vk+Vy+Va, for example, 260V, is applied between the corresponding scan electrode Y1, Y2, ..., or Yn and a selected address electrode Am. Here, the negative voltage -Vk-Vy higher than the negative voltage -Vk is applied to each of the scan electrodes Y1, Y2, ..., Yn, to thereby relatively lower the address voltage Va. When the negative voltage -Vp is applied when the facing discharge occurs, the facing discharge ceases. As shown in FIG. 7, positive(+) wall-charges are accumulated under the scan electrodes 231, 232 of a selected pixel. Reference numerals of FIG. 7 which are the same as those of FIG. 2 indicate identical elements.

In the first sustaining discharge interval (K-L), 0 V is applied to the address electrodes Am, a pulse of the negative(-) voltage -Vk is applied to the common electrodes X, and a pulse of the positive(+) voltage Vs is applied to scan electrodes Y1, Y2, ..., Yn. And thereby, surface discharges occurs in the selected pixels. As shown in FIG. 8A, negative(-) wall-charges are accumulated under scan electrodes 231, 232 of the selected pixel, and positive(+) wall-charges are accumulated under the common electrodes 241, 242. Reference numerals of FIG. 8A which are the same as those of FIG. 2 indicate identical elements. When a

surface discharge occurs in the selected pixel, plasma is formed in a gas layer of a corresponding region, and a luminescent material 22 is excited by a UV-ray, to emit light.

In the second sustaining discharge interval, 0 V is applied to the address electrodes Am, a pulse of the positive(+) voltage Vs is applied to the common electrodes X, and a negative(-) voltage -Vk is applied to the scan electrodes Y1, Y2, ..., Yn. And thereby, surface discharges occur in the selected pixels. As shown in FIG. 8B, positive(+) wall-charges are accumulated under the scan electrodes 231, 232 of the selected pixel, and negative(-) wall-charges are accumulated under the common electrodes 241, 242. Reference numerals of FIG. 8B which are the same as those of FIG. 2 indicate identical elements. when a surface discharge occurs in the selected pixel, plasma is formed in a gas layer of a corresponding region, and the luminescent material 22 is excited by a UV-ray, to thereby emit light. The operations of the first and second sustaining discharge steps (interval K-N) are repeated during a predetermined sustaining discharge interval (K-Q), to maintain illumination of the selected pixel.

FIG. 9 shows voltage waveforms applied to electrodes according to a plasma display panel driving method based on the other embodiment of the present invention. Comparing FIG. 9 to FIG. 4, the voltage waveform applied to the common electrodes X is changed in the reset interval (A-G). The operation in the address and sustaining discharge interval (G-Q) is same as that described above. So, referring to FIG. 9, the operation in only the reset interval (A-G) will be explained.

In the first reset interval (A-B), 0 V is applied to the Address electrodes Am and the common electrodes X, and a pulse of the negative(-) voltage -Vk are applied to the scan electrodes Y1, Y2, ..., Yn. Accordingly, the wall-charges in the pixels selected in a previous sub-field are removed. Also, as shown in FIG. 6A, positive(+) wall-charges are accumulated in a protective layer 26 under each of the scan electrodes 231, 232 of the pixel selected in the previous sub-field, and negative(-) wall-charges are accumulated in the protective layer 26 under the common electrodes 241, 242. Meanwhile, wall-charges are not accumulated in a pixel region not selected from the previous sub-field.

In an additional reset interval (B-C), 0 V, a pulse of the positive(+) voltage +Vs, and a pulse of the negative(-) voltage -Vk are applied to the address electrodes Am, the scan electrodes Y1, Y2, ..., Yn, and the common electrodes X, respectively. Accordingly, the wall-charges accumulated in the first reset interval (A-B) are removed.

In the second reset interval (C-D), 0V is applied to the address electrodes Am and the common electrodes X, and a a pulse of the positive(+) voltage Vw for facing discharge, for example, 180 V, are applied to the scan electrodes Y1, Y2, ..., Yn. Accordingly, a facing discharge occurs between the address electrodes Am of pixels where wall-charges are accumulated in the first reset interval (A-B), that is, the pixels selected from the previous sub-field, and the scan electrodes Y1, Y2, ..., Yn. Meanwhile, a facing discharge does not occur between the address electrodes Am of pixels where wall-charges are not accumulated in the first reset interval (A-B), that is, the pixels not selected from the previous sub-field, and the scan electrodes Y1, Y2, ..., Yn. As shown in FIG. 6B, negative(-) wall-charges are accumulated in the protective layer 26 under the scan electrodes 231, 232 of each pixel selected from the previous sub-field, and the positive(+) wall-charges are accumulated in a luminescent material 22 of the address electrodes Am. Here, positive(+) wall-charges are accumulated in the protective layer 26 under the common electrodes 241, 242. Meanwhile, wall-charges are not accumulated in a pixel region not selected from the previous sub-field.

In the third reset interval (E-F), 0 V is applied to the address electrodes Am and the common electrodes X, and a pulse of the negative(-) voltage -Vk is applied to the scan electrodes Y1, Y2, ..., Yn. The operation of the third reset interval is performed relatively quickly, so that the pulse width of the negative(-) voltage -Vk applied to the scan electrodes Y1, Y2, ..., Yn, is relatively short. The operation of the third reset interval (E-F) is sequentially performed again. Accordingly, as shown in FIG. 6C, the wall-charges of the pixels selected from the previous sub-field are removed. Also, the additional reset interval (B-C) is repeated after the the third reset interval (E-F), and thererby, most of the remnant wall charges can be removed. Nevertheless, there are residual wall charges on the address electrodes Am in the reset interval (A-G), and thereby the second

voltage Va+Vk+Vy applied in the address interval (G-K) can be lowered.

Industrial Applicability

As described above, according to a driving method of a surface discharge type alternating current plasma display panel of the present invention, the wall charges to be removed are accumulated by the facing discharge in the reset step. Accodingly, the light of relatively low brightness is emitted from the pixels unselected in each sub-field, to thereby increase the contrast of the display screen. Also, there are residual wall charges on only the address electrodes after the reset step, and thereby the voltage applied in the address interval can be lowered.

The present invention is not limited to the illustrated embodiment and many changes and modifications can be made within the scope of the invention by a person skilled in the art.

What is claimed is:

1. A method of driving a surface discharge plasma display panel having a first substrate and a second substrate space apart and facing each other, and common electrodes, scan electrodes, and address electrodes arranged between said first and second substrates, said common electrodes being arranged in parallel with said scan electrodes, said address electrodes being arranged orthogonal to said common electrodes and said scan electrodes to form respective intersections which each define a corresponding pixel, comprising:

a resetting step of applying a first voltage between the scan electrodes and the address electrodes to accumulate wall charges in the respective pixel by a facing discharge, and removing the wall-charges accumulated by the facing discharge;

an addressing step of applying a second voltage between a corresponding scan electrodes and selected address electrodes so that a facing discharge occurs, to form wall-charges in the selected pixels; and

a sustained discharging step of applying a third alternating-current voltage between the scan electrodes and the common electrodes so that a surface discharge occurs in the selected pixels.

2. The driving method of claim 1, wherein the resetting step includes:

a first resetting step of applying a fourth voltage between the scan electrodes and the common electrodes, and thereby remove remnant wall-charges from a previous sub-field, said fourth voltage has an opposite polarity to a voltage applied last in the sustained discharging step;

a second resetting step of applying said first voltage between the scan electrodes and the address electrodes, and thereby cause the facing discharge in the respective pixel selected from a previous sub-field;

a third resetting step of applying a fifth voltage between the scan electrodes and the address electrodes, and thereby remove wall-charges accumulated by the facing discharge, said fifth voltage has an opposite polarity to said first volatge and lower than said first voltage.

3. The driving method of claim 2, wherein said third resetting step is shorter than the first and second resetting steps.

4. The driving method of claim 4, wherein said third resetting step is repeated.

Abstract

A driving method of a surface discharge plasma display panel includes a resetting step, an addressing step and a sustained discharging step. In the resetting step, a first voltage is applied between the scan electrodes and the address electrodes to accumulate wall charges in the respective pixel by a facing discharge, and the wall-charges accumulated by the facing discharge are removed. In the addressing step, a second voltage is applied between a corresponding scan electrodes and selected address electrodes so that a facing discharge occurs, to form wall-charges in the selected pixels. In the sustained discharging step, a third alternating-current voltage is applied between the scan electrodes and the common electrodes so that a surface discharge occurs in the selected pixels.

FIG. 1

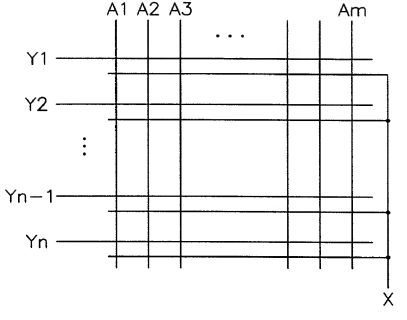

A1 A2 A3
Am
Y1
Y2
Yn−1
Yn
X

FIG. 2

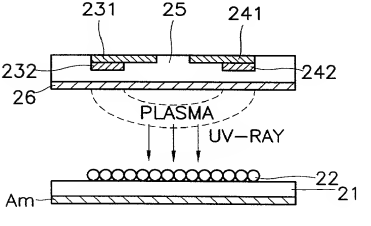

231
25
241
232
242
26
PLASMA
UV−RAY
22
21
Am

FIG. 3 (PRIOR ART)

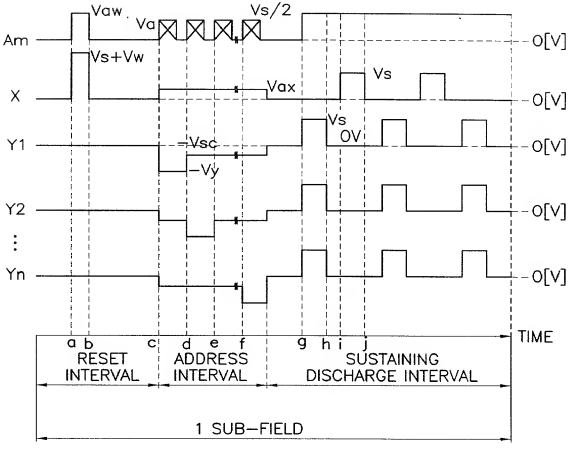
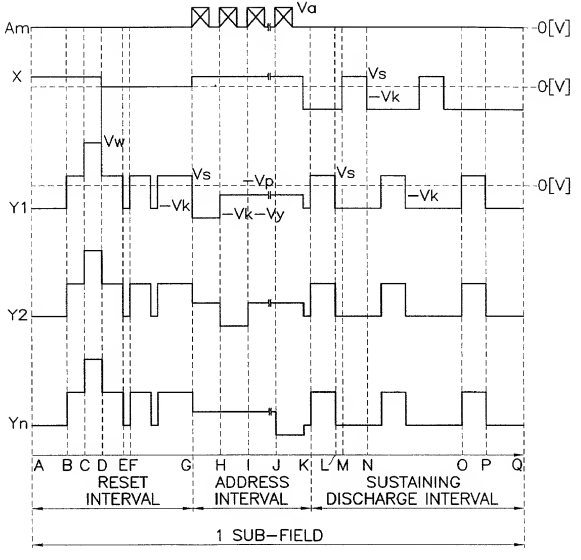


FIG. 4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Am
0[V]
X
Vs
-Vk
0[V]
Vw
Vs
-Vp
Vs
Y1
-Vk
-Vk-Vy
-Vk
0[V]
Y2
Yn
A B C D EF G H I J K L M N O P Q
RESET INTERVAL
ADDRESS INTERVAL
SUSTAINING DISCHARGE INTERVAL
1 SUB-FIELD

FIG. 5

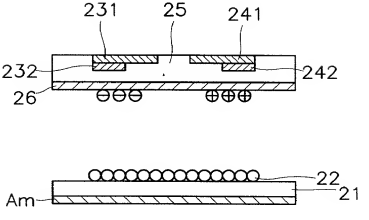


FIG. 6A

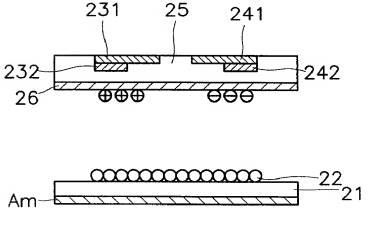


FIG. 6B

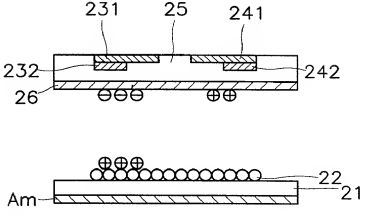


FIG. 6C

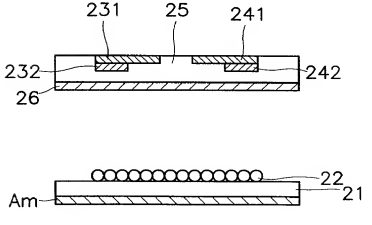


FIG. 7

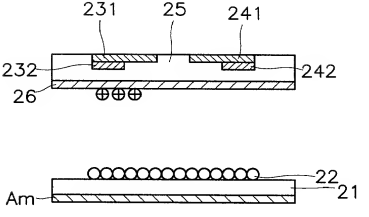


FIG. 8A

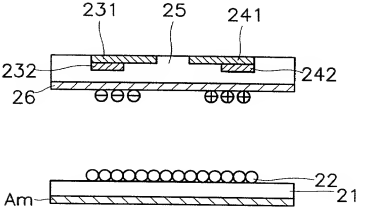


FIG. 8B

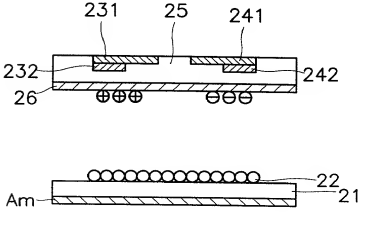
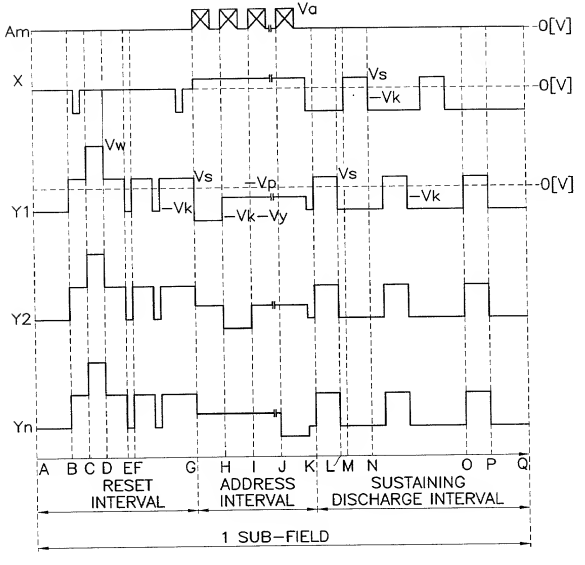


FIG. 9


Va
Am
0[V]
X
Vs
-Vk
0[V]
Vw
Vs
-Vp
Vs
Y1
-Vk
-Vk
-Vk-Vy
-Vk
0[V]
Y2
Yn
A B C D EF G H I J K L M N O P Q
RESET INTERVAL
ADDRESS INTERVAL
SUSTAINING DISCHARGE INTERVAL
1 SUB-FIELD

Docket No 2729-038

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that.

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if pl
names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled
METHOD OF DRIVING SURFACE DISCHARGE PLASMA DISPLAY PANEL
, the specification of which

[ ] is attached hereto [X] was filed on 17/4/1998 As International Application No. and was amended on
(if applicable) PCT/KR98/00091

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amen
by any amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, C
of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any fore
application(s) for patent or inventor's certificate, or Section 365(a) of any PCT international application which designated at least
country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certifi
having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	
Number	Country	Day/Month/Year filed	Yes	No
97-14995	Korea	22/04/1997	X	

I hereby claim the benefit under 35 USC §119(e) of any United States provisional application(s) listed below.

Prior Provisional Application(s):

Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of
PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of
application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragrap
Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Fe
Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing
of this application:

Prior U. S. Application(s):

Serial No.	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and I
are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so
are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful
statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) and/or agent(s): Allan M. Lowe, Reg. No. 19,641, Israel Gopstein, Reg. No. 27,333; Benjamin J. Hauptman, Reg. No. 29,310, Kenneth M. Berner, Reg. No. 37,093 and Michael G. Gilman, Reg. No. 19,114; all of

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with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all future correspondence should be addressed to them.

****

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